



LOCATION, FEES AND REGISTRATION

Surf to WWW.IDESA-TRAINING.ORG for all course details.

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Dates and locations:
www.idesa-training.org



Advanced Digital Physical implementation flow



TARGET AUDIENCE

This course targets Professors, Post-docs and PhD students within European academia who are involved in the planning and presentation of lectures and lab exercises for engineering master curricula

OBJECTIVES

The participants will become familiar with the changes introduced in the IC design flows for advanced deep-submicron technology nodes. The 90 nm technology will be the baseline for the EDA-platform used, using relevant process parameters and IP-libraries.

The course will create a deeper understanding of the issues involved by providing lectures by experts in the field. The course will also build hands-on experience. State-of-the-art EDA tools and relevant design exercises will bring the participants to a level at which they can confidently face future design flow challenges introduced by the 65 nm and 45 nm process characteristics and constraints.

PREREQUISITES

Course participants should be familiar with IC design and should have a basic understanding of the IC design flow applied for the 180 nm and 130 nm nodes.

LOCATION

This 5-day course will tour Europe starting September 2010 and will be organized at several academic locations.



DAY 1**LECTURE 1: INTRO: WHAT ARE THE NEW CHALLENGES TO DESIGN 90NM SOCS****LECTURE 2: DESIGN ENVIRONMENT & TOOL CHAIN****M. WILMOTT — STFC**

This session introduces 90nm digital IC design, giving an overview of the topics that are covered throughout the remainder of the course, including: Technology Changes, Design and Verification, Test Strategy, Low Power Techniques, Physical Implementation and Signoff Technologies. The morning concludes with an introduction to the 90nm EDA tools and implementation flows.

LECTURE 3 + LAB: DESIGN SYNTHESIS**M. WILMOTT — STFC**

This session looks in detail at modern synthesis technologies: including topographical synthesis (with physical constraints), low power optimisation (both static and dynamic power), and Scan Test (with compressed scan).

DAY 2**LECTURE 4: POWER AWARE DESIGN****N. GAUR — IMEC**

To reduce power, chip architects and IC designers must understand and be able to take advantage of the many different techniques and technologies available for power reduction.

LECTURE 5: DESIGN PLANNING**S. O'LOUGHLIN — IMEC**

This lecture discusses chip-level floorplanning & power network design. The impact of implementing different low power techniques is presented, including topics such as voltage islands, isolation cells, MTCMOS, etc.

LECTURE 6: LIBRARY ANALYSIS AND MANAGEMENT (STANDARD CELL, IO, MEMORY)**LECTURE 7: IP INTEGRATION AND MANAGEMENT (HARD-, SOFT-, ANALOG IP)****N. GAUR — IMEC**

The correct choice of libraries and IP is crucial to achieve the desired IC performance. This session includes topics to help understand cell library basics such as operating conditions, min-max corners and multi Vth, as well as tips for choosing IP vendors.

LAB 2: DESIGN PLANNING**S. O'LOUGHLIN — IMEC**

DAY 3**LECTURE 8 + LAB: LOW POWER FLOW****N. GAUR — IMEC + W. KUZMICZ — WUT**

Dynamic & leakage power minimization and how to use a unified power intent specification to assure coherence over the design flow and to allow verification of the power features.

LECTURE 9: PHYSICAL SYNTHESIS - PLACEMENT AND OPTIMISATION**S. O'LOUGHLIN — IMEC**

How do we move from the synthesized gate level description and floorplan to a physical layout, and how do we ensure that our design will meet our performance, area and power targets?

LECTURE 10: CLOCK TREE SYNTHESIS**S. O'LOUGHLIN — IMEC**

How does clock tree synthesis work at 90nm especially in the light of multi voltage designs, gated clocks and other low power techniques and what is the impact on skew and insertion delay?

DAY 4**LECTURE 11: PHYSICAL SYNTHESIS – DESIGN FOR TEST (DFT)****N. GAUR — IMEC**

DFT techniques & scan chain re-ordering and their impact on the design.

LECTURE 12: PHYSICAL SYNTHESIS – MULTIMODE AND MULTICORNER**N. GAUR — IMEC**

How to make sure that the chip is going to work in all the different operation modes (functional, BIST, scan test, ...) and, when using multiple voltages in multiple corners. This session also explains MMMC flow implementation using a unified power intent file (e.g. CPF/UPF).

LECTURE 13: PHYSICAL SYNTHESIS – ROUTING TO GDS2**S. O'LOUGHLIN — IMEC**

How to route clock and signals nets and to analyze and repair crosstalk violations.

LAB 4: PHYSICAL SYNTHESIS**N. GAUR — IMEC + W. KUZMICZ — WUT**

DAY 5**LECTURE 14: IR DROP ANALYSIS****N. GAUR — IMEC**

IR drop analysis and its impact on chip timing, and methods to reduce IR drop.

LECTURE 15: ON-CHIP VARIATION AND STATISTICAL STATIC TIMING ANALYSIS**N. GAUR — IMEC****LAB 5: SIGNOFF ANALYSIS INCLUDING DYNAMIC GATE IR ANALYSIS AND STATIC TIMING****ANALYSIS INCLUDING SIGNAL INTEGRITY****N. GAUR — IMEC + W. KUZMICZ — WUT****LECTURE 16: SIGN-OFF****N. GAUR — IMEC**

Sign-off extraction and all the analyses needed to be sure that the chip will work. What to do if there are violations. What can we do early in the flow to make sure not to get any surprises?

LECTURE 17: DESIGN FINISHING & LAYOUT VERIFICATION**S. O'LOUGHLIN — IMEC**

Design rule and layout verification checks, dummy fill and chip finishing.

LECTURE 18: TAPE-OUT**N. GAUR — IMEC**

Tape-out issues, data preparation & documentation.