Tutorial 11

Using the “System Layout Module”
For industrial feasibility evaluation
Simulating propagation delay in inverter chain loaded with capacitive and resistive systems
Calculating the « Static Noise Margin » of 6T-SRAM cells
Using the randomization effects in order to evaluate the impact of variability of device parameters on electrical performance of circuits.
Inverter Speed Evaluation, incl. RC Line

Inverter 1  Inverter 2  Inverter N

\[ R_{\text{line}} \]

\[ C_{\text{load}} \]

\[ L_{G} \]

\[ M_{X} \]

\[ L_{\text{int}} \]
Ex-1: Computing Inverter Delay including interconnections

- Input here
  1. the number of stages
  2. timing information
  3. period of the input signal
  4. R and C values for the BEOL
  5. click compute

Signal output at stage 2

Input signal

Signal output at last stage (here 4)
Delay at Vdd/2 extraction
Ex-2: Computing SRAM SNM

Click here to start the SRAM evaluation

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When boxes are unchecked, only 1 SNM is computed.

Note: to bring the Compute Menu, just right-click here in the graph windows.
**Computing SRAM SNM**

If none of the box are checked → 1 cell calculation

Calculation precision

If at least one of the box is checked → several cell calculation with « random » variation on selected parameters

---

**Compute SNM & AVt**

**SRAM**

- Enable random Lg  \( \sigma = 0.1 \) nm
- Enable random Doping
- Enable random \( \chi / T_s i \)  \( \sigma = 0.1 \) nm
- Enable random \( \Phi_{m} \)  \( \sigma = 0.1 \) mV
- Enable random \( K_{ni} \)  \( \sigma = 0.1 \)
- Only half cell calculation
  - \( n_{tr} = 100 \)
  - \( \delta_{V} = 0.01 \)

**Compute**

---

**Extracted results**

- SNM: 277.25 mV
- SNM avg: 0.00 mV
- \( \sigma_{SNM} \): 13.52 mV

**Graphs**

- Vr (V) vs VI (V)

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If « Only half cell calculation » is checked, computation time will be divided by 2, but butterfly curve will always be symmetric.

If « Only half cell calculation » is not checked, computation time butterfly can be assymetric.
Check boxes to generate variability

Choose the number of generated SNM. Check « enable Symetrical curve » to compute only a half cell, or uncheck to generate the whole cell variability

After calculation, statistical data are available

Choose the data to display
Tutorial 12

Inverter Delay
Objective: evaluate the inverter’s delay as a function of layout of transistors, interconnection length, and process variability

Content

- Background Elements
  - Parasitic Capacitances of MOSFETs
  - Input and Output capacitance of an Inverter chain
- Ex-1: Influence of N/P Ratio on Inverter’s delay
- Ex-2: Optimal N/P ratio in the case of a boosted PMOS transistor
- Ex-3: Impact of process variability on the « worst-case » inverter’s speed
- Ex-4: Influence of interconnect wire length on speed performance
Bibliography


Capacitance definition

- $C_{gc}$: on-state gate-to-channel cap
- $C_{gb\_off}$: off-state gate to substrate cap.
- $C_{ov}$: overlap cap
- $C_{of}$: outer-fringe cap
- $C_{if}$: inner-fringe cap
- $C_{pcca}$: poly to contact plug cap.
- $C_{j}$: junction cap
- $C_{corner}$: corner cap, from the gate overlay to S/D

Ref.: Lan Wei, STMicroelectronics-STANFORD Univ. Collaboration pgm. & Lan Wei, VLSI TSA 2009
### Caps for a Single Device

<table>
<thead>
<tr>
<th></th>
<th>Cd (on)</th>
<th>Cg(on)</th>
<th>Cg(off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cgc</td>
<td>Gate-to-channel</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Cgb_off</td>
<td>Gate-to-sub</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Cov</td>
<td>Gate overlap</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Cof</td>
<td>Gate outerfringe</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Cif</td>
<td>Gate inner fringe</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Cpcca</td>
<td>Gate to plug</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Ccorner</td>
<td>Corner cap</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Cj</td>
<td>Junction cap</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

- $C_{gb\_off}$ and $C_{if}$ are shielded by the channel in on-state.
- $C_{gc}$ is not seen by drain node in on-state, due to pinch-off.

*Ref.: Lan Wei, STMicroelectronics-STANFORD Univ. Collaboration pgm. & Lan Wei, VLSI TSA 2009*
Caps for an Inverter Chain

\[ C_L = \left( C_{GDP1} + C_{GDN1} \right) \times 2_{Miller} + C_{jDP1} + C_{jDN1} + C_{\text{interco}} + \]

\[ C_{\text{GBP2} \text{, OFF}} + 0.25 C_{\text{GBP2, ON}} + C_{\text{GDP2}} + C_{\text{GDN2}} + 0.25 C_{\text{GBN2, OFF}} + 0.75 C_{\text{GBN2, ON}} + C_{\text{GSN2}} \]
Capacitance for an Inverter Chain

\[ C_{tot} = C_{dg} \cdot Miller + C_j + \left(0.25C_{g\_off} + 0.75C_{g\_on}\right) \cdot FO + C_{interconnect} \]

\[
= \left(C_{ov} + C_{of} + C_{pcca} + C_{corner}\right) \cdot Miller + C_j \\
+ \left[0.25\left(C_{gc} + C_{ov} + C_{of} + C_{pcca} + C_{corner}\right) + 0.75\left(C_{ov} + C_{of} + C_{pcca} + C_{corner}\right)\right] \cdot FO \\
+ C_{interconnect}
\]
With MASTAR5

- **MASTAR System Layout Function**
  - Calculate $\tau_{1fF}$ by full waveform calculation
  - $\tau_{FO1}, \tau_{FO3}$ are estimated by

$$
\tau_{FO1(3)}_{\text{adjusted}} = \tau_{1fF} \cdot \frac{C_{\text{inverter}_FO1(3)}}{1fF}
$$

- where, $C_{\text{inverter}_FO1(3)}$ is calculated by the new models

- **Different design possibilities are analyzed**
  - Wn/Wp ratios, high driving-capable PMOS
Ex-1 : N/P Ratio (1)

1. Open the system profile basline.xsy
2. Note the ratio between NMOS’s Ion and PMOS’s Ion : $727/396 = 1.83$
3. Set $W_p=720\text{nm}$ and $W_n=360\text{nm}$
4. Perform the calculation of the inverter’s delay.
5. Write down the $T_{p FO1}$ value
Ex-1 : N/P Ratio (2)

- Calculate the delay of a FO1 inverter for the following configurations
- plot the delay as a function of WP/WN
- Q: Explain the behavior

<table>
<thead>
<tr>
<th>WN</th>
<th>WP</th>
<th>WP/WN</th>
</tr>
</thead>
<tbody>
<tr>
<td>360</td>
<td>180</td>
<td>0.5</td>
</tr>
<tr>
<td>360</td>
<td>360</td>
<td>1</td>
</tr>
<tr>
<td>360</td>
<td>720</td>
<td>2</td>
</tr>
<tr>
<td>240</td>
<td>720</td>
<td>3</td>
</tr>
<tr>
<td>180</td>
<td>720</td>
<td>4</td>
</tr>
</tbody>
</table>
### Ex-1 : N/P Ratio - Answer

<table>
<thead>
<tr>
<th>WN</th>
<th>WP</th>
<th>WP/WN</th>
<th>TpFO1 (ps)</th>
<th>Tp/fF</th>
<th>Ctot (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>360</td>
<td>180</td>
<td>0.5</td>
<td>22.12</td>
<td>15.53</td>
<td>1.42</td>
</tr>
<tr>
<td>360</td>
<td>360</td>
<td>1</td>
<td>17.86</td>
<td>9.97</td>
<td>1.79</td>
</tr>
<tr>
<td>360</td>
<td>720</td>
<td>2</td>
<td>17.21</td>
<td>6.8</td>
<td>2.53</td>
</tr>
<tr>
<td>240</td>
<td>720</td>
<td>3</td>
<td>19.43</td>
<td>8.5</td>
<td>2.29</td>
</tr>
<tr>
<td>180</td>
<td>720</td>
<td>4</td>
<td>21.87</td>
<td>10.11</td>
<td>2.16</td>
</tr>
</tbody>
</table>

- **Optimal Intrinsic delay is** 6.8ps
- **C at optimum speed is** 2.53fF

Inverter Delay (ps)

Min~1.8
- Calculate the delay of a FO1 inverter for the following configurations
- plot the delay as a function of WP/WN
- Q: Explain the behavior
Ex-2 : N/P Ratio with Boosted pMOS

<table>
<thead>
<tr>
<th>WN</th>
<th>WP</th>
<th>WP/WN</th>
<th>TpFO1 (ps)</th>
<th>Tp/fF</th>
<th>Ctot (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>360</td>
<td>180</td>
<td>0.5</td>
<td>14.2</td>
<td>9.97</td>
<td>1.42</td>
</tr>
<tr>
<td>360</td>
<td>360</td>
<td>1</td>
<td>12.19</td>
<td>6.8</td>
<td>1.79</td>
</tr>
<tr>
<td>360</td>
<td>720</td>
<td>2</td>
<td>12.62</td>
<td>4.99</td>
<td>2.53</td>
</tr>
<tr>
<td>240</td>
<td>720</td>
<td>3</td>
<td>14.72</td>
<td>6.44</td>
<td>2.29</td>
</tr>
<tr>
<td>180</td>
<td>720</td>
<td>4</td>
<td>16.92</td>
<td>7.82</td>
<td>2.16</td>
</tr>
</tbody>
</table>

Intrinsic delay is still 6.8ps
But C at optimum speed is now 1.79fF

Inverter Delay (ps)

Min~1.0
Ex-3 : Delay and Variability

- **Objective**: Study the impact of technology variability on device performance/speed
- **Context**
  - Every technology feature intrinsic variations due to process variation or stochastic variations
    - Transistor gate length, $3\sigma = 12\% \times L_{\text{gate}}$ (ITRS)
    - Stochastic variation of electrode workfunction due to random dopant fluctuations (in Poly-Silicon electrode) or metallic grain orientation fluctuation (in metallic electrode), $\sigma \sim 10\text{mV}$
    - Random Fluctuation of transistor’s channel doping [Mizuno *et al.* VLSI 93]
    - Junction depth variation …
    - …
  - This will impact the $V_{\text{th}}$ and the $I_{\text{dsat}}$ of transistors and therefore create a statistical distribution of inverter’s delay
Ex-3 - Worst Case « Process » Simulation

![Simulation Interface](image)

**Static parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>100</td>
</tr>
<tr>
<td>L</td>
<td>5</td>
</tr>
<tr>
<td>VDD</td>
<td>5.0V</td>
</tr>
<tr>
<td>VSS</td>
<td>0V</td>
</tr>
<tr>
<td>VGS</td>
<td>0V</td>
</tr>
<tr>
<td>ID</td>
<td>10mA</td>
</tr>
</tbody>
</table>

**Dynamic parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>1MHz</td>
</tr>
<tr>
<td>C</td>
<td>10pF</td>
</tr>
<tr>
<td>R</td>
<td>1kΩ</td>
</tr>
</tbody>
</table>

![Graph](image)

**Extracted results**

- Voltage: 3.6V
- Current: 10mA

**Inverter Simulation**

- Stage = 6
- Delay = 0.7ns

**Randomization**

- Enable random Lg, sig = 2.4V
- Enable random Doping, sig = 3mV
- Enable random Vth, sig = 10mV
- Enable random Km, sig = 0.1V
- Enable random Riff, sig = 1kΩ

**Simulation Parameters**

- Vgs = Vdd - Vth
- Rd = Vdd - Vgs
- Iout = (Vdd - Vgs) / Rd

**Conclusion**

- The simulation results show a low power consumption and high performance.

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Q: Use the following table to analyse the scaling of inverter’s delay as well as the scaling of the worst case delay (i.e delay + 3σ).

| Tab 1: Summary of ITRS2005 device parameter and generated circuit parameters used in this study. |
|---|---|---|---|---|---|---|
| Half Pitch (nm) | 80 | 65 | 45 | 32 | 22 | 16 |
| Lphys logic (nm) | 32 | 25 | 18 | 13 | 9 | 6 |
| Architecture | Bulk | Bulk | FDSG | FDSG | DG | DG |
| Ion n (μA/μm) | 1020 | 1200 | 1815 | 2200 | 2900 | 2744 |
| Ion p(μA/μm) | 510 | 600 | 907.5 | 1100 | 1450 | 1372 |
| SRAM size (μm²) | 0.76 | 0.50 | 0.24 | 0.12 | 0.06 | 0.03 |
| WPU (nm) | 80 | 65 | 45 | 32 | 22 | 16 |
| LPU (nm) | 32 | 25 | 18 | 13 | 9 | 6 |
| LPD (nm) | 32 | 25 | 18 | 13 | 9 | 6 |
| WPD (nm) | 120 | 98 | 68 | 48 | 33 | 24 |
| LPG (nm) | 43 | 34 | 24 | 17 | 12 | 8 |
| WPG (nm) | 80 | 65 | 45 | 32 | 22 | 16 |
| Inverter |  |  |  |  |  |  |
| Wn (nm) | 80 | 65 | 45 | 32 | 22 | 16 |
| Wp (nm) | 160 | 130 | 90 | 64 | 44 | 32 |
| C_interco (aF/μm) | 186.7 | 165.5 | 153.3 | 131.3 | 121.3 | 102.2 |
| R_interco (Ohm/μm) | 1.8 | 3.9 | 11.2 | 24.8 | 62.1 | 143.4 |

After F. Boeuf et al., T-ED 2008
Answer: as devices are scaled down, they are more and more sensitive to variability sources. As a consequence, after 50nm half-pitch generation, the worst case delay is scaling slower (4% faster/year) than the average delay (17% faster/year).

After F. Boeuf et al., T-ED 2008
Ex-5 Impact of Wire Length on Delay

L,R negligible

T. Skotnicki & F. Boeuf
Ex- 5 Impact of Wire Length on Delay

Q1: Calculate the propagation delay after the stage 2 for L varying between 0 and 50 µm. What is the maximum wire length possible?
Q2: How to go beyond this value?

Assume R = 2.0 Ohm/µm
Assume C = 200 aF/µm
(corresponding to 2005 ITRS values)

Answer to Q1:

<table>
<thead>
<tr>
<th>L (µm)</th>
<th>R (Ohm)</th>
<th>C (F)</th>
<th>Delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8.72</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>2.00E-16</td>
<td>9.87</td>
</tr>
<tr>
<td>10</td>
<td>20</td>
<td>2.00E-15</td>
<td>20.28</td>
</tr>
<tr>
<td>20</td>
<td>40</td>
<td>4.00E-15</td>
<td>31.32</td>
</tr>
<tr>
<td>50</td>
<td>100</td>
<td>1.00E-14</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Ex- 5 Impact of Wire Length on Delay

L=1µm

L=10µm

L=20µm (Signal starts to be deformed = Lmax)

L=50µm (Signal cannot propagate correctly)

Answer to Q1 (con’t)
Ex- 5 Impact of Wire Length on Delay

Answer to Q2

Increase Wn and Wp to achieve higher transistor’s drive current. E.g. multiply Wn and Wp by 2.0

L=20µm

L=40µm  New Lmax is above 40µm
Q: Use the following table to analyse the scaling of inverter’s delay across the ITRS roadmap, for a wire length scaling between 0.68x per year and 0.8x per year.
Ex- 6 : Inverter’s Delay and Metal Line Resistance accross the Roadmap

Answer

For 0.68x, delay is properly scaling as inverter delay with a FO1 load.

For 0.8x, delay is not scaling at all with the technology!

Fig. 2: Intrinsic device delay (CVI) and Inverter delay for different loading capacitance as a function of technology pitch.
Bibliography


- **Is a “Power Optimized” Roadmap Realistic for High Performance Applications?** Frederic Boeuf and Thomas Skotnicki, In Extented Abstracts of SSDM 2007 (JSAP CAT AP071239), pp. 258-259
Tutorial 13: Device Scaling
Starting from a relatively old device profile, we will carry out a series of modifications to end up with a scaled-down up-to-date device. The following analysis and modifications will be considered:

- Pocket implants
- SCE and DIBL
- Junction depth reduction
Ex. 1:
STARTING DEVICE PROFILE
Analysis of problems
« IDESA Start »
Starting device profile (IDESA Start)
Starting device profile – analysis

- Note that the channel doping is constant \(2 \times 10^{17} \text{ cm}^{-2}\)
- The threshold voltage drops rapidly down
- Already at \(L_{gate}=137\text{nm}\), \(V_{th sat off}\) reads at no more than 150mV that corresponds to \(I_{off}=10\text{nA/µm}\)
- For many applications this is already difficult to tolerate
- Not to mention that such long \(L_{gate}\) would have a detrimental effect on the density of integration
- Remember that this « IDESA Start » profile corresponds (except for \(L_{gate}\)) to a LOP 65nm CMOS, where the gate should read at 65nm or below

- The first point we will analyse is thus how to make the gate shorter without lowering the \(V_{th sat off}\)?
Ex. 2
USE OF POCKET IMPLANTS
% a commonly used technique enabling gate shortening in CMOS technologies
Reverse Short Channel Effect due to “POCKETS” or “HALLOS”:

Idea: instead of increasing the substrate doping uniformly, that would lead to junction leakage (here), we increase it very locally (here) that prevents SCE and DIBL without leading to huge junction leakage.

Ions implanted with dose $C_{poches}$ and energy $\rightarrow R_p, \Delta R_p, \Delta R_l$.
USE OF POCKET IMPLANTS

Pocket implantation conditions

Gain in Lgate minimum thanks to pockets
POCKETS – analysis

- Note that instead of the same Vthsat, the Ioff (leakage is not the same as without pockets.
- This is because of relaxation in the Subthreshold Slope

\[
S = \frac{kT}{q} \ln \left( 0 \right) \left( 1 + \frac{C_{\text{dep}} + \varepsilon_{\text{Si}} T_{\text{ox}} X_j}{C_{\text{ox}} \varepsilon_{\text{ox}} L_{\text{el}} L_{\text{el}}} \left( 1 + \frac{3 T_{\text{dep}}}{4 L_{\text{el}}} \right) \right)^{-1} \sqrt{2 \varepsilon_{\text{Si}} \left( \phi_d + V_{SB} \right)}
\]

- The major source of this relaxation in SS comes from the \( \frac{C_{\text{dep}}}{C_{\text{ox}}} \) term = \[\frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \times \frac{T_{\text{ox}}}{T_{\text{dep}}} \]
- Pockets increase the doping that leads to a decrease in

\[
T_{\text{dep}} = \sqrt{\frac{2 \varepsilon_{\text{Si}}}{q N_B} \left( \phi_d + V_{SB} \right)}
\]

- That leads to an increase in SS (68 without pockets and 91 with)
Ex. 3

HOW TO REDUCE $L_{gate,min}$ FURTHER?

% REDUCTION OF SCE and DIBL

(note that in the last example with pockets, $SCE=135mV$ and $DIBL=193mV$, whereas before, i.e. without pockets they were $SCE=26mV$ and $DIBL=40mV$. This means that application of pockets was not totally capable of cancelling the relaxation in Electrostatic Integrity of the device that is caused by the reduction of the gate from 137 nm to 53 nm)
Bothe SCE and DIBL lower the barrier that appears to the electrons wishing to move from source to drain, and therefore both lead to more leakage current $I_{off}$.

SCE – Short Channel Effect

DIBL – Drain Induced Barrier Lowering
SCE, DIBL & RSCE IMPACT ON Vth-L:

\[ V_{th} = V_{th, L \to \infty} + RSCE - SCE - DIBL \]
SCE & DIBL DEPEND ON RATIOS, RATHER THAN ON VALUES OF PARAMETERS:

\[ V_{th} = V_{th,L \to \infty} - SCE - DIBL \]

\[ SCE = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox - el}}{L_{el}} \frac{T_{dep}}{L_{el}} \phi_d \]

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox - el}}{L_{el}} \frac{T_{dep}}{L_{el}} \]

\[ T_{dep} = \sqrt{\frac{2 \varepsilon_{Si} \phi_D}{qN_B}} \]
Ex. 4
REDUCTION OF SCE and DIBL
%
Via reduction of junction depth $X_j$
REDUCTION OF JUNCTION DEPTH

Xj reduced from 20nm to 12nm

Improved SCE and DIBL thanks to reduced Xj

Gain in Lgate minimum thanks to Xj reduction
Tutorial 14:
High-K/Metal Gate Stack
DESCRIPTION

- Cancellation of polydepletion
- Gate oxide reduction
- Readjustment of pockets
- New $L_{\text{gate,minimum}}$
- Gate leakage
- Introduction of HK gate dielectric
Ex. 1
REDUCTION OF SCE and DIBL %
Via reduction of Oxide Thickness

(note that the effective gate dielectric thickness is a summ of the physical gate dielectric thickness, of the polydepletion and of the so called « Dark space » - see next slide)
POLYDEPLETION & “DARK SPACE”:

\[ T_{\text{ox\_el}} = T_{\text{ox\_phys}} + \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{Si}}} T_{\text{poly}} + \frac{\varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{Si}}} T_{\text{dark\_space}} \]

N+Poly-gate  SiO2  Si-P-substrate

3D electrons in the gate

2D electrons in the gate in accumulation

2D electrons in the gate in depletion

3D electrons in the channel

Darkspace in the channel

Polydepletion

T. Skotnicki & F. Boeuf

STMicroelectronics
IMPLICATIONS OF Tox REDUCTION

\[ V_{th,\infty} = (\Phi_m - \Phi_S) + \frac{qN_{ss}}{C_{ox}} + 2\phi_F + \frac{\sqrt{2\varepsilon_{Si}qN_B(\phi_d + V_{SB})}}{C_{ox}} \]

where

\[ C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \]

Note that reduction of Tox not only leads to reduced SCE and DIBL but also to a reduction in long-channel threshold voltage that therefore needs to be compensated by increased doping or readjusted gate work function.
IMPLICATIONS OF POLYDEPLETION (Metallic gate)

SCE and DIBL are reduced. Metallic gate cancels poly depletion. Same Vth is maintained due to readjustment of the gate workfunction.

**Table:**

<table>
<thead>
<tr>
<th>Performance</th>
<th>Threshold volt</th>
<th>Dynamic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ion = 7.39 × 10⁻⁵ A/µm</td>
<td>Vthsat = 257.78 mV</td>
<td>CgVdd/iod = 1.75 mV</td>
</tr>
<tr>
<td>Ion = 2.67 × 10⁻⁸ A/µm</td>
<td>Vthbog = 230.54 mV</td>
<td>t_invert = 3.52 ps</td>
</tr>
<tr>
<td>Ion = 7.39 × 10⁻⁵ A/µm</td>
<td>Vthsat = 0 mV</td>
<td>FpGc = 3.24 × 10⁻⁵ A/µm</td>
</tr>
<tr>
<td>Ion = 1.06 × 10⁻⁸ A/µm</td>
<td>Vthbog = 307.78 mV</td>
<td>Cg = 1.00 × 10⁻¹ F/µm</td>
</tr>
<tr>
<td>Ion = 7.39 × 10⁻⁵ A/µm</td>
<td>Vthsat = 2.20 mV</td>
<td>Cg = 1.00 × 10⁻¹ F/µm</td>
</tr>
<tr>
<td>Ion = 3.48 × 10⁻⁸ A/µm</td>
<td>Vthbog = 34.81 mV</td>
<td>Cg = 1.00 × 10⁻¹ F/µm</td>
</tr>
<tr>
<td>Ion = 50.00 A/µm</td>
<td>Vthsat = 34.81 mV</td>
<td>Cg = 1.00 × 10⁻¹ F/µm</td>
</tr>
<tr>
<td>Ion = 50.00 A/µm</td>
<td>Vthsat = 34.81 mV</td>
<td>Cg = 1.00 × 10⁻¹ F/µm</td>
</tr>
</tbody>
</table>

**Graph:**

- SCE: 79.41 mV
- DIBL: 113.4 mV

---

**Notes:**

- **Metallic gate cancels poly depletion.**
- **Same Vth is maintained due to readjustment of the gate workfunction.**

---

**Context:**

- **SCE** (Subthreshold Characteristics): Reduced due to metallic gate cancellation of poly depletion.
- **DIBL** (Differential Subthreshold swing): Also reduced, ensuring constant Vth.

---

**Technical Details:**

- **Performance Metrics:** Ion, Ion saturation, Vth, etc., showing significant improvements.
- **Capacitance:** Calculated for different states (poly depletion, metallic gate) with specific values provided.
- **Graphs:** Show Vth vs. Lgate, highlighting the impact of different gate materials and their implications on device performance.
SCE and DIBL are further reduced.

Reduced also leads to gate leakage.

Same Vth is maintained due to readjustment of the gate workfunction.
Ex. 2
READJUST POCKETS and TRADE ALL IMPROVEMENTS in SCE and DIBL AGAINST FURTHER REDUCTION OF Lgate, minimum
NEW IMPROVED TECHNOLOGY!

Ioff is back to its initial value.

But Lgate is X4 shorter !!!

Pocket implantation conditions readjusted.
Ex. 3

PROBLEM OF $I_{\text{gate}}$

INTRODUCING H-K GATE DIELECTRIC

(note that once we have thinned $\text{Tox}$ from 1.8nm to 1.2nm, the $I_{\text{gate}}$ leakage increased from $1.18 \times 10^{-1}$nA/$\mu$m to $8.33 \times 10^{2}$nA/$\mu$m thus exceeding the channel leakage $I_{\text{off}} = 1.02 \times 10^{1}$nA/$\mu$m. This situation is not tolerable!)

---

T. Skotnicki & F. Boeuf
MASTAR Igate MODEL (very good):

\[
I_g[A/cm^2] = 1.44 \times 10^5 \times \exp(-4.02 U_g[V]^2 + 13.05 U_g[V]) \times \exp(-1.17 \times T_{ox}[Å])
\]

Simulation data:
- Hauser, NCSU, UQUANT model

T. Skotnicki & F. Boeuf
High-K PRINCIPLE:

\[ C_g = \frac{K}{T_{\text{die}}l} \]

\[ J_g \propto \exp\left(-T_{\text{die}}l \sqrt{\Phi b}\right) \]

If \( K \) and \( T_{\text{die}}l \) increase in parallel,
- \( C_g \) is conserved
- \( J_g \) decreases rapidly

In practice we always keep a thin pedestal oxide at the dielectric-Silicon interface. The H-K material is deposited on top of the pedestal oxide.
Huge reduction in $I_{off}$, from $8.33 \times 10^2$ nA/µm to $1.96 \times 10^0$ nA/µm thanks to HK

If EOT=constant is selected, MASTAR will automatically calculate the required TIF (Technology Improvement Factor=$I_{gate, SiO2}/I_{gate, H-K}$) from the settings given by the user.
The final device profile we have achieved presents largely shorter gate (reduced X4).
All other parameters (SCE, DIBL, SS, Ioff, Igate,off, etc) are however at their maximal tolerable values.
This prevents further scaling down.
Also Variability and Speed of the technology suffer from these border-line values.
Therefore other solutions, breakthrough like, will have to be considered to pursue scaling.
We will first explain Variability and Impact of DIBL on performance, and next.
Consider more robust device structures enabling further scaling.
Tutorial 15:

DEVICE VARIABILITY
Ex. 1
Derivation of the threshold voltage fluctuation model
And
its discussion
discreteness of matter starts to play. To assess the impact of random number of dopants in the channel let us calculate the derivative:

\[
\delta V_{th} = \frac{1}{C_{ox}} \frac{\delta Q_c}{\delta n_c} \delta n_c = \frac{q T_{ox}}{\varepsilon_{ox} W L} \delta n_c
\]

where \( Q_c \) is the channel depletion charge and \( n_c = N_c T_{dep} W L \) is the number of dopants in the depleted channel region. If we suppose now, [13], that the number of dopants in the channel undergoes the Gaussian distribution, with a standard deviation \( \sigma = \delta V_{th} \), we have from the properties of the Gaussian distribution \( \sigma^2 = n_c \), or:

\[
\delta n_c = \sqrt{n_c} = \sqrt{N_c} \sqrt{\frac{2 \varepsilon_s \varepsilon_0}{q N_c} \Phi_d W L}
\]

that after substitution in (10) gives:

\[
\delta V_{th} = \sqrt{\frac{2 \varepsilon_s \varepsilon_0 q^3 N_c \Phi_d}{\varepsilon_{ox} \varepsilon_0} T_{ox}} \frac{1}{\sqrt{L W}} \equiv A_{vt} \frac{1}{\sqrt{L W}}
\]

STRONG CHANNEL DOPING (e.g. POCKETS) ENHANCES Vth FLUCTUATIONS

=> UNDOPED CHANNEL WITH MID-GAP GATE (ON THIN FILM SOI/SON) MAY BE A REMEDY

REF.: T. Cochet, T. Skotnicki et al., ESSDERC'99
VARIABILITY - FLUCTUATIONS:

$$\delta V_{th} = \frac{4\sqrt[4]{4\varepsilon_s q^3 \varphi_F}}{2\varepsilon_{ox}} \frac{T_{ox}}{\sqrt{L_{el}W}} \sqrt[4]{N_{ch}}$$

A 4.2 nm MOSFET in production 2023

Electron concentration

8k-MOSFET ARRAY, Tox=11nm, Nch=7.1e16cm-3

Courtesy of A. Asenov, Glasgow Univ., UK

T. Mizuno et al., IEEE TED, Nov. 1994
Line Edge Roughness (LER) and Poly Grains (PGG) vs Random Dopant Distribution (RDD) – RDD is the dominant effect!

A. Cathignol et al., EDL, 2008 (ST)

Courtesy Prof. A. Asenov Glasgow U.
Fluctuations – IMPACT ON LOGIC and on SRAM

\[ \delta V_{th} = \frac{4\sqrt{2\varepsilon_s \varepsilon_0 q^3 N_c \Phi_d}}{\varepsilon_{ox} \varepsilon_0} T_{ox} \frac{1}{\sqrt{LW}} \equiv A_{vt} \frac{1}{\sqrt{LW}} \]

Huifang Qin

SNM w/o process spread

SNM with process spread

Courtesy Prof. A. Asenov

T. Skotnicki & F. Boeuf
Ex. 2
Device Variability as function of its size
The statistical distribution of Vt is narrow with Nominal MOSFETs.
The statistical distribution of $V_t$ is large with Scaled Down MOSFETs.
Tutorial 16:

SRAM VARIABILITY
Ex. 1
Analysis of SRAM SNM (Static Noise Margin) in function of Vdd (supply voltage)
LP IS DIFFICULT

The SNM (Static Noise Margine) vanishes when lowering the Vdd, thus preventing correct voltage scaling! As a result the Vdd has been stagnating in LP technologies around 1.1V (see next slide).

VARIABILITY IS BEHIND THE VDD CLUMSY SCALING AND THUS BEHIND THE « POWER CRISIS »

Evolution of VDD (LSTP)

- 5V plateau
- 1.2V plateau
- 1.1V and ~1V plateau ???

10 years of « constant-field » scaling from 5V to 1.2V (x 0.7 per node)

Year of production (ITRS)

Volt:
- 700 (1980)
- 500 (1992)
- 250 (1998)
- 180 (2000)
- 120 (2002)
- 65 (2007)
- 45 (2010)
- 32 (2015)
CALCULATING THE EFFECT OF VANISHING SNM WITH MASTAR (1)
Ex. 2
Analysis of SRAM SNM (Static Noise Margine) in function of the cell size
The SNM (Static Noise Margin) vanishes when reducing dimensions, thus preventing technology scaling down! As a result the Lgate in LP technologies is relaxed w/r to the scaling theory.

CALCULATING THE EFFECT OF VANISHING SNM WITH MASTAR (2)

All dimensions Scaled by X0.7
All dimensions scaled again by X0.7
If L and W are scaled $X0.7$ for each CMOS generation, the $A_{vt}$ has also to be improved $X0.7$ in order to maintain the voltage fluctuation constant.

\[ \delta V_{th} = \frac{4 \sqrt{2 \varepsilon_s \varepsilon_0 q^3 N_c \Phi_d}}{\varepsilon_{ox} \varepsilon_0} T_{ox} \frac{1}{\sqrt{LW}} \equiv A_{vt} \frac{1}{\sqrt{LW}} \]
Avt reduction is very difficult with Bulk

Conflict with cell-leakage

Conflict with electrostatics when L shrink

Conflict when Area shrink

\[ \sigma_{VT} = \left( \frac{\sqrt[4]{4q^3 \varepsilon_{Si} \phi_B}}{2} \right) \frac{T_{ox}}{\varepsilon_{ox}} \frac{\sqrt{N}}{\sqrt{W_{eff} L_{eff}}} \]

P. Stolk at al., T-ED 1998 (NXP)

Two solutions appear:

1) Tox – conflict with cell leakage can be alleviated when using HK dielectrics

2) N – conflict with electrostatics can be removed when going to FDSOI or FinFET
Ex. 3
Analysis of Vmin (SRAM sustaining voltage) – comparison between doped channel (Bulk) and undoped channel (FDSOI)
## SRAM: Minimum Operating Voltage

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tolerable Die Fail</td>
<td>0.0001</td>
<td>0.0001</td>
<td>0.0001</td>
<td>0.0001</td>
<td>0.0001</td>
<td>0.0001</td>
</tr>
<tr>
<td>Memory Size(Mbits)</td>
<td>8</td>
<td>16</td>
<td>32</td>
<td>64</td>
<td>128</td>
<td>256</td>
</tr>
<tr>
<td>Tolerable Bit Fail</td>
<td>1.25E-11</td>
<td>6.25E-12</td>
<td>3.13E-12</td>
<td>1.56E-12</td>
<td>7.81E-13</td>
<td>3.91E-13</td>
</tr>
<tr>
<td>Required SNM/σSNM</td>
<td>6.8</td>
<td>6.85</td>
<td>6.95</td>
<td>7</td>
<td>7.15</td>
<td>7.25</td>
</tr>
</tbody>
</table>

### Vmin reduction

C. Shin et al., SOI Conference’09

T. Skotnicki & F. Boeuf
LESS VARIABILITY W. SOI - EXPLANATION:

Ref.: Denis Flandre, UCL Louvain-La-Neuve, BE

\[ \frac{\sigma_{Vt(SOI)}}{\sigma_{Vt(Bulk)}} = \left( \frac{Na_{SOI}}{Na_{Bulk}} \right)^{1/4} = (1/100)^{1/4} \approx 1/3 \]

X100 reduction in doping corresponds to X3 reduction in \(\sigma_{Vth}\) or in Avt !!!
Variability and LP SRAM:

Bulk: $\text{Avt} \approx 3.3, \; V_{dd,\text{nom}} = 0.9V$

FDSOI: $\text{Avt} = 1.4$

Data: F. Bœuf

Bulk: $\text{Avt} = 2$
FDSOI: $\text{Avt} = 1.4$

We gain 150 mV in $V_{\text{min}}$

World record by LETI!

O. Weber et al. IEDM 2008 (LETI)

FDSOI/UTBOX

$V_{\text{min}} \approx 0.6V$

$V_{\text{min}} \approx 0.75V$
CONTINUITY OF SRAM SIZE SCALING:

- 6T-SRAM bitcell is composed by:
  - 2 PMOS transistors
  - 4 NMOS transistors

- Area scales as 0.5X per generation

From PullNano Project (EU/IST)

F. Arnaud et al, VLSI 03 (ST)
F. Boeuf et al, VLSI 2005 08 (C2 Alliance)
H.S. Yang et al, IEDM 07 (TSMC)
B.S. Haran et al, IEDM 08 (IBM)

F. Boeuf, 2009 VLSI SC
Tutorial 17:

DEVICE SPEED – IMPACT OF DIBL
Effective Current \( (I_{eff}) \) as metric of speed (performance)

**SWITCHING TRAJECTORY WHEN CHARGING / DISCHARGING THE LOAD**

\[
\text{switching speed } \propto \frac{I_{eff}}{C_{load}V_{dd}}
\]

\[I_{on} \text{ is NOT a speed indicator}\]

\[I_{eff} \text{ IS A GOOD SPEED INDICATOR}\]

\[
I_{eff} = \frac{1}{2} \left[ I\left(V_G = \frac{V_{dd}}{2}; V_D = V_{dd}\right) + I\left(V_G = V_{dd}; V_D = \frac{V_{dd}}{2}\right) \right]
\]

Ref.: M.H. Na et al., IEDM 2002, p.121.
HOW DOES DIBL IMPACT PERFORMANCE ($I_{eff}$)

- Long channel

- SCE – Short Channel Effect

- DIBL – Drain Induced Barrier Lowering

T. Skotnicki & F. Boeuf
PERFORMANCE (IEFF) depends on DIBL –NEW !!!

**Equation:**

\[ I_D = \beta \times V_d \left( V_g - V_{th} - \frac{1}{2} V_d \right) \]

- \( \Delta V_{th} \) - DIBL
- \( \Delta V_{th} \) - DIBL
- Techno w/o DIBL
- Techno w. DIBL
- \( V_{dd} \)
- \( V_{dd}/2 \)
- \( V_d \)
- \( I_{eff \ w. \ DIBL} < I_{eff \ w/o \ DIBL} \)

**Graph:**
- Green arrow indicates same \( I_{on} \), same \( I_{off} \)
- Red arrow indicates \( \Delta V_{th} \) - DIBL
- Adjust \( V_{th} \)
- Huge leakage !!!
Ex. 1

Compare $I_{eff}$ (speed) between two technologies having same $I_{on}$ and $I_{off}$ but different DIBL
How much improvement due to DIBL reduction?

Same Ion & Ioff
But DIBL = 142 mv in one techno and 0 mV in another
+40% in Ieff
means +40% in speed !!!

186.5
261

+40% in Ieff

switching speed $\propto \frac{I_{eff}}{C_{load}V_{dd}}$
Tutorial 18:

III-V high mobility channels
Better mobility and higher limiting velocity lead to an increase in the transistor Ion current.

However, lower density of states in the inversion layer (larger Dark Space) leads to reduced inversion density, and relaxed SS, SCE and DIBL.

Also the higher dielectric constant of III-V materials lead to an increase in SS, SCE and DIBL.

Only making a sum of these constructive and destructive effects permits to assess the real interest of III-V channel materials.
High $\mu/\text{vsat} \sim \text{Small } E_g \sim \text{High } \varepsilon$

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>Eff. Electron mass</th>
<th>Bandgap (eV) at 300K</th>
<th>Dielectric constant</th>
<th>Electron bulk mobility (cm$^2$/Vs)</th>
<th>Saturation velocity ($10^7$ cm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InSb</td>
<td>0.014</td>
<td>0.17</td>
<td>15.9</td>
<td>77000</td>
<td>5</td>
</tr>
<tr>
<td>InAs</td>
<td>0.023</td>
<td>0.36</td>
<td>12.</td>
<td>30000</td>
<td>3.5</td>
</tr>
<tr>
<td>GaSb</td>
<td>-</td>
<td>0.68</td>
<td>14.8</td>
<td>5000</td>
<td>-</td>
</tr>
<tr>
<td>InP</td>
<td>-</td>
<td>1.27</td>
<td>12.1</td>
<td>4500</td>
<td>-</td>
</tr>
<tr>
<td>GaAs</td>
<td>0.063</td>
<td>1.43</td>
<td>11.5</td>
<td>8000</td>
<td>1.2</td>
</tr>
<tr>
<td>Ge</td>
<td>1.59/0.081</td>
<td>0.66</td>
<td>16</td>
<td>3600</td>
<td>0.6</td>
</tr>
<tr>
<td>Si</td>
<td>0.98/0.19</td>
<td>1.12</td>
<td>12</td>
<td>1350</td>
<td>1</td>
</tr>
</tbody>
</table>

Virtual III-V (~InGaAs): $\mu_{\text{eff}} \times 10$, $\text{vsat} \times 3$, $\varepsilon \times 1.25$, $T_{\text{inv}} + 2$ up to +6.5Å

T. Skotnicki & F. Boeuf
How do $\varepsilon$ & Dark Space impact DIBL and SS in III-V’s (1)

$$T_{\text{inv}} = T_{\text{ox}} + DS.\varepsilon_{\text{ox}}/\varepsilon_s$$

$$DIBL = 0.80 \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{\text{inv}}}{L_{el}} \frac{T_{\text{dep}}}{L_{el}} V_{DS}$$

$$T_{\text{dep}} = \sqrt{\frac{2\varepsilon_{\text{Si}}\phi_D}{qN_B}}$$

$$SS = \frac{kT}{q} \ln(10) \left[ 1 + \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \frac{T_{\text{inv}}}{T_{\text{dep}}} + \frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} \frac{T_{\text{inv}}}{L_{el}} \frac{X_j}{L_{el}} \left( 1 + \frac{3}{4} \frac{T_{\text{dep}}}{L_{el}} \right) \sqrt{1 + \frac{V_{DS}}{\Phi_d}} \right]$$

How do $\varepsilon$ & Dark Space impact DIBL and SS in III-V's (2)

- $\varepsilon$ +3 (+25%)
- Tinv+6.5A (+59%)
- Reference (Si)

Graph showing:
- DIBL (mV) vs $I_{off}$ (nA/$\mu$m) for different currents: 10nA/$\mu$m, 100nA/$\mu$m, 2µA/$\mu$m
Ex. 1
Estimating impact of constructive effects on III-V MOSFET speed
Inspite of higher mobility, III-V may be slower!

Readjust gate workfunction to same Ioff

Positive Impact on Ion

Negative Impact on speed

DIBLx2

μX10 VsatX3
CONCLUSIONS

- At low Vdd the impact of bad electrostatics is particularly strong
- III-V materials present very good transport properties, but much relaxed electrostatics (DIBL and SS)
- At nominal transistor length and low Vdd, the destructive effects, due to electrostatics, preveil over the constructive effects, due to better transport properties
- Consequently, the overall impact of the replacement of Silicon by III-V materials may be negative in terms of speed
- Still remains true, that lagging the transistor length one node behind nominal permits higher speed than Bulk (see biblio, next slide), but leads to lower density of integration
Bibliography

Tutorial 19:

DEVICE STRUCTURES - FDSOI
FDSOI especially with thin BOX shows much improved SCE, DIBL and SS

Such a FDSOI on thin BOX is also called UTBB (Ultra Thin Body and BOX) SOI

We will explain why UTBB shows better electrostatics and benchmark it against BULK using MASTAR

We will also show how to transform the Bulk transistor current model into a model valid for UTBB SOI

Comparison of current and inverter speed (via Ieff) will be carried out with MASTAR for Bulk and UTBB SOI
Ex. 1

WHY DOES UTBB SOI BETTER THAN BULK IN TERMS OF ELECTROSTATICS?
FDSOI devices on SOI Wafers

Krivokapic et al., IEDM 2002 (AMD)
K. Cheng et al., VLSI 2009 (IBM)
C. Fenouillet-Beranger et al., unpublished (ST/LETII)
N. Sugii et al., IEDM 2008 (Hitachi)
R. Chau et al., IEDM 2001 (Intel)
C. Fenouillet-Beranger et al., IEDM 2009 (ST/LETII)

SOTB
DST
Hybrid FDSOI
FDSOI
BULK

T. Skotnicki & F. Boeuf
WHY DOES THE PLANAR MOSFET FAIL?

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

Suppose: \( L_{el} = \frac{2}{3} L_g \)

\[ 2.4 \left( 1 + \frac{3^2}{4^2} \right) \frac{1}{20} \frac{3}{4} 1V = 140 mV \]

WHY DOES THE UTB SOI/SON DO BETTER?


\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

Suppose: \( T_{si} = \frac{1}{3}L_g \) & \( L_{el} = \frac{2}{3}L_g \)

\[ 2.4 \left( 1 + \frac{1^2}{2^2} \right) \frac{1}{20} \frac{1}{2} 1V = 75mV \]

REF.: T. Skotnicki, invited paper ESSDERC 2000, pp. 19-33, edit. Frontier Group
Electrostatics of UTB SOI

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left(1 + \frac{X_j^2}{L_{el}^2}\right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

\[ X_j \rightarrow T_{Si} \]
\[ T_{dep} \rightarrow T_{Si} + \lambda T_{box} \]

\[ \lambda = 0.21 \left(1 + \tanh\left(1.50 \frac{T_{box}}{L_{el}} - 1\right)\right) \left(1 + 0.09 \frac{T_{box}}{L_{el}}\right) \frac{L_{el}}{T_{box}} \]

For Tbox in the range of 10-50nm, \( \lambda \approx 0.3 \)

C. Fenouillet-Beranger, et al., SOI Conference 2003
T. Skotnicki et al. IEEE EDL, March’88 & IEDM’1994

Closed symbol: TCAD simulation
Open symbol: MASTAR

NMOS FDSOI
Tox 1nm Vdd 1V
Tsi 5nm

Lg 30nm
Lg 40nm

STMicroelectronics
T. Skotnicki & F. Boeuf
COMPARE BULK LAST POINT (HK and pockets) WITH FDSOI

Note huge DIBL!
We will pass to FDSOI making the following changes (next slide):

1) Replace $X_j$ by $T_{si}$ (suppose 6nm)
2) Replace $T_{dep}$ by $T_{si} + 0.3T_{box}$ (suppose $T_{box}=10$nm)
WE CAN MIMIC FDSOI MODIFYING BULK PARAMETERS:

Tsi is set to 6nm, thus Xj is also set to 6nm.

Note improvement in DIBL!

Tdep=9nm (=Tsi+λTbox =6nm+0.3x10nm) is obtained by artificially increasing the doping Nbulk and readjusting Workfunction.
For convenience of use, all these and other changes aiming at mimicking the FDSOI behavior with the Bulk models, are already programmed in MASTAR.

The modifications are slightly more complex (see next slide) and calibrated on experimental data.

Nevertheless, pushing the button « SOI » gives results similar to what we have obtained manipulating the Bulk model manually.

See next slide.
TECHNOLOGY FLAVORS-TRANSLATION TO MASTAR:

Apply when you push button BULK, DG or SOI.

<table>
<thead>
<tr>
<th>Preferences applied on Interface Profile</th>
<th>Preferences applied in calculation module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kfield</td>
<td>Kd</td>
</tr>
<tr>
<td>--------</td>
<td>----</td>
</tr>
<tr>
<td><strong>BULK</strong></td>
<td></td>
</tr>
<tr>
<td><strong>SOI</strong></td>
<td></td>
</tr>
<tr>
<td><strong>DG</strong></td>
<td></td>
</tr>
</tbody>
</table>

Color Check: <-> 1 <-> 1 <-> 85 <-> 0.8 <-> 0.64

*Attention: in this version, Eeff models account for the SOI and DG specificity => no need for Kfield correction

\[ T_{DIBL}^{dep} = T_{dep} + \rho \left( \frac{3(L - X_j)T_{box}}{L - X_j + 3T_{box}} \right) \]

\[ SCE = \zeta_2 \frac{\varepsilon_{si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{elec}^2} \right) \frac{T_{ox_{-}eot}}{L_{elec}} \frac{T_{dep}}{L_{elec}} V_{th} \]

\[ DIBL = \zeta_1 \frac{\varepsilon_{si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{elec}^2} \right) \frac{T_{ox_{-}eot}}{L_{elec}} \frac{T_{DIBL}^{dep}}{L_{elec}} V_{th} + \beta \Delta_{DIBL} \]
FDSOI USING BUTTON « TECHNOLOGY FLAVORS »!

Bulk FDSOI By « press button » SOI

FDSOI By «manual parameter manipulation»
Ex. 2
INVERTOR SPEED – COMPARISON BULK AND FDSOI
SPEED IMPROVEMENT WITH FDSOI!

+33% in I_{eff} means +33% in speed when passing from BULK to FDSOI!!

switching speed \propto \frac{I_{eff}}{C_{load}V_{dd}}
Ex. 3
INVERTOR SPEED – FDSOI with Forward Body Bias
FinFET’s INCOMPATIBILITY W. BODY-BIAS whereas FDSOI with thin BOX is !

FDSOI = 2D

FinFET w. SEPARATE GATES LOST ADVANTAGE IN DIBL !

FinFET w. COMMON GATE

Body-Bias EASY As on Bulk

Body-Bias IMPOSSIBLE Since GATE=BACK-BODY

Body-Bias STILL IMPOSSIBLE Since Gate(N+1)=Body(N)

And NO ROOM for CONTACTS

Thin Silicon film

T. Skotnicki & F. Boeuf
SPEED IMPROVEMENT WITH FDSOI and Forward Body Bias!

FDSOI (directly after push button « SOI » and adjusting Tsi)

FDSOI Adjusted to same Ioff as Bulk

BULK

With FBB

+FBB

+82% in Ieff means +82% in speed

switchingspeed ω (Ieff / Cload Vdd)
Tutorial 20:

DEVICE STRUCTURES- DG / FinFET
DG structures (eg FinFET) show much improved SCE, DIBL and SS

We will explain why DG/FinFET shows better electrostatics

We will also show how to transform the Bulk transistor current model into a model valid for DG/FinFET

Comparison of current and inverter speed (via Ieff) will be carried out with MASTAR for Bulk and DG/FinFET
DOUBLE GATE DEVICES:

Tied gates (number of channel > 2) TRIGATE

Tied Gates side-wall conduction: DELTA, FINFET, OMEGAFET,…

Independently switched gates planar conduction

Vertical conduction

Tied gates planar conduction: DG SON
FinFET - STATE OF THE ART

FinFET structure in a dense array with CPP=80nm and Fin pitch = 50nm

Kang–Sematech
IEDM 2006 [12]

Collaert–IMEC
VLSI-TSA 2007 [13]

IBM Alliance ,
Albany 2010

Shang–IBM
VLSI 2006 [15]

Lenoble–STM/IMEC
VLSI 2006 [16]
WHY DOES THE Double-Gate DO BETTER?

\[ DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left( 1 + \frac{X_j^2}{L_{el}^2} \right) \frac{T_{ox}}{L_{el}} \frac{T_{dep}}{L_{el}} V_{DS} \]

Suppose: 
- \( T_{si} = \frac{1}{3} L_{g} \)
- \( L_{el} = \frac{2}{3} L_{g} \)
- \( X_j = \frac{1}{2} T_{si} \)
- \( T_{dep} = \frac{1}{2} T_{si} \)
- \( X_j = \frac{1}{6} L_{g} \)
- \( T_{dep} = \frac{1}{6} L_{g} \)

\[ 2.4 \left( 1 + \frac{3^2}{12^2} \right) \frac{1}{20} \frac{1}{4} \ 1V = 32mV \]

REF.: T. Skotnicki, invited paper ESSDERC 2000, pp. 19-33, edit. Frontier Group
TECHNOLOGY FLAVORS-TRANSLATION TO MASTAR:

Apply when you push button BULK, DG or SOI.

Preferences applied on Interface Profile

<table>
<thead>
<tr>
<th>Kfield</th>
<th>Kd</th>
<th>Slope</th>
<th>ζ1</th>
<th>ζ2</th>
</tr>
</thead>
<tbody>
<tr>
<td>BULK</td>
<td>1</td>
<td>85</td>
<td>0.8</td>
<td>0.64</td>
</tr>
<tr>
<td>SOI</td>
<td>1</td>
<td>0.5</td>
<td>75</td>
<td>0.77</td>
</tr>
<tr>
<td>DG</td>
<td>1</td>
<td>65</td>
<td>0.35</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Preferences applied in calculation module

<table>
<thead>
<tr>
<th>α</th>
<th>Xi</th>
<th>Tdep</th>
<th>β</th>
<th>σ</th>
<th>Cj0 (IF/µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Xi</td>
<td>Tdep</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0.16</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Color Check: <> 1 <> 1 <> 85 <> 0.8 <> 0.64

*Attention: in this version, Eeff models account for the SOI and DG specificity ⇒ no need for Kfield correction

\[
\begin{align*}
T_{dep}^{DIBL} &= T_{dep} + \rho \left( \frac{3( L - X_j) T_{ox}}{L - X_j + 3T_{ox}} \right) \\
SCE &= \zeta_2 \frac{\varepsilon_{si}}{\varepsilon_{ox}} \left( 1 + \frac{X_{j}^2}{L_{elec}^2} \right) \frac{T_{ox\_eot}}{T_{elec}} \frac{T_{dep}}{L_{elec}} V_{th} \\
DIBL &= \zeta_1 \frac{\varepsilon_{si}}{\varepsilon_{ox}} \left( 1 + \frac{X_{j}^2}{L_{elec}^2} \right) \frac{T_{ox\_eot}}{L_{elec}} \frac{T_{DIBL}}{L_{elec}} V_{th} + \beta \Delta_{DIBL}^{DIBL}
\end{align*}
\]
Ex. 1
INVERTOR SPEED – COMPARISON BULK AND DG/FinFET
SPEED IMPROVEMENT WITH FinFET!

+47% in $I_{\text{eff}}$ means +47% in speed when passing from BULK to FinET!!

$\text{switchingspeed} \propto \frac{I_{\text{eff}}}{C_{\text{load}}V_{\text{dd}}}$
CONCLUSIONS (FDSOI & DG/FinFET)

- FDSOI as well as DG structures (eg FinFET) show much improved SCE, DIBL and SS
- These features lead to very strong performance improvement, especially at low Vdd (Low Power applications)
- Without Body Bias, FinFET gives larger improvement than FDSOI due to better electrostatics
- But FinFET is not compatible with Body Bias, whereas FDSOI is and provides better Body Factor than Bulk
- Therefore with Forward Body Bias, FDSOI gives even better speed than FinFET!